Master level Internship: Formalizing Hardware Security Mechanisms: a new HDL for modular hardware proofs

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Context The security of applications eventually depends on the security of all the abstractions layers they are built upon. The application itself may contain some hardening techniques, it may benefit from isolation provided by the operating system (OS), and it may also be secured through the use of hardware security mechanisms. For critical applications, formal methods (e.g. static analysis, model checking, formal proof) have been successfully applied at the source code level (e.g. Astrée, VST), at the compiler level (e.g. CompCert [7]), at the OS level (seL4 [6], CertiKOS [5]), and more recently at the hardware level (e.g. Kami [4], Kôika [3]).

Several of these approaches are based on the Coq proof assistant,[1] which allows for formal definition of semantics and proofs. The Coq proof assistant is a program that helps building proofs and rigorously checks that the proofs are correct. The Kôika language is a high-level hardware design language (HDL) embedded in Coq, together with a verified compiler to Verilog. Thanks to this approach, one can design a circuit in the high-level HDL (Kôika) and generate from that a description in a low-level HDL (Verilog) that standard hardware tools can use to synthetise the circuit on FPGA. The authors proved that the compiler preserves the semantics of Kôika.

In the SUSHI group, we aim at proving security properties guaranteed by hardware/software mechanisms. We proposed an approach to prove security properties about Kôika designs. This requires to compile Kôika designs to an intermediate representation more suitable than the Kôika representation to formal verification. We proved that this compilation is correct and successfully apply this methodology to prove the security of a shadow stack[2] in a RISC-V processor [2]. This forms a foundation for proving more complex security mechanisms.

Our current approach consists in automatically compiling Kôika designs to a more explicit representation, and then manually proving the properties of interest on this representation. This approach can still be improved. First, our approach is monolithic. Indeed, the semantics of Kôika deals with complex interactions between so-called atomic rules inspired by BlueSpec [1], and actions in different rules may conflict with each other and induce global effects. It is therefore non-trivial to reason modularly about Kôika designs. Second, our approach consists in compiling Kôika designs to a more explicit representation, about which we managed to prove our properties of interest. This means that the proof we end up writing is not about the Kôika design itself, but about something automatically generated from it, which makes proofs very fragile (not robust to changes in the design).

Other HDLs exist which, like Kôika, enable to write higher level code and compile to Verilog/VHDL. Among these HDLs, Chisel relies on the Scala language for the "meta-programming" aspects, and compiles into an intermediate representation called FIRRTL (Flexible Intermediate Representation for RTL).[3] Unlike Kôika, the Chisel language has a more straightforward semantics (e.g. no rule cancellation) and should be more amenable to modular reasoning.

Internship The goal of the internship is to contribute to the formalization of the FIRRTL language in Coq, already started in our team.

Here are the main steps of the internship:

- get familiar with Coq and the Kôika language;
- get familiar with the RISC-V processor written in that language and the proof methodology that we used in [2];
- contribute to the formalization of the FIRRTL language in Coq;
- propose some proof techniques for hardware designs written in that language. These techniques should allow for modular reasoning.
- translate the proofs of [2] into this new framework, hopefully showing that the new framework makes proofs easier to write.

[1] https://coq.inria.fr
[2] https://en.wikipedia.org/wiki/Shadow_stack
[3] https://www.chisel-lang.org/

Required skills or interests The candidate should be familiar with the Coq proof assistant. Knowledge about hardware design languages (e.g. Chisel, FIRRTL, and Verilog/VHDL) is a plus.

Institute The internship will take place at CentraleSupélec in Rennes, France, in the soon-to-be-created SUSHI Inria team[4]. This team is part of the IRISA laboratory.[5] The internship will be advised by Pierre Wilke and Guillaume Hiet.

Practical aspects The internship will last 5 months, starting from February, 2024. The intern will receive a "gratification" of 609€ per month. Housing options may be available on campus, or close to the campus.

This internship could be followed by a Ph.D. thesis on similar subjects.

References

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[2] Matthieu Baty et al. "A Generic Framework to Develop and Verify Security Mechanisms at the Microarchitectural Level: Application to Control-Flow Integrity". In: *36th IEEE Computer Security Foundations Symposium, CSF 2023, Dubrovnik, Croatia, July 10-14, 2023*. IEEE, 2023, pp. 372–387. DOI: 10.1109/CSF57540.2023.00029. URL: https://doi.org/10.1109/CSF57540.2023.00029.

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[7] Xavier Leroy and Sandrine Blazy. "Formal verification of a C-like memory model and its uses for verifying program transformations". In: *Journal of Automated Reasoning* 41.1 (2008), pp. 1–31. URL: http://xavierleroy.org/publi/memory-model-journal.pdf.

[4] The team is currently CIDRE: https://team.inria.fr/cidre/

[5] https://www.irisa.fr/en